

What Is Claimed Is:

1. An ATM switch, comprising:
 - one or more input side circuit interfaces;
 - one or more output side circuit interfaces; and

5 an ATM core switch for outputting cells inputted thereto from said input side circuit interface or interfaces to said output side circuit interface or interfaces;

each of said output side circuit interfaces feeding back a cell number accumulated for each virtual channel to a 10 corresponding one of said input side circuit interfaces;

each of said input side circuit interfaces shaping the rate of cells based on the feedback from a corresponding one of said output side circuit interfaces so that a peak cell rate total value of virtual channels which belong to a virtual path 15 may not exceed a peak cell rate of the virtual path;

each of said output side circuit interfaces controlling, based on the cell number accumulated for each virtual channel, so that the peak cell rate of the virtual path to which the virtual channels belong may not exceed the peak cell rate total 20 value of the virtual channels which belong to the virtual path.
2. An ATM switch as claimed in claim 1, wherein each of said input side circuit interfaces includes a physical layer processing section which terminates a cell, and an input virtual channel cell rate control section for receiving the cell 25 terminated by said physical layer processing section and controlling the rate of cell for each virtual channel based

on the feedback.

3. An ATM switch as claimed in claim 2, wherein each of said output side circuit interfaces includes an output virtual channel cell rate control section for storing a cell number 5 accumulated for each virtual channel, an output virtual path cell rate control section for controlling the cell rate for each virtual channel based on the cell number accumulated in said output virtual channel cell rate control section, and a physical layer section for outputting a cell from said output 10 virtual channel cell rate control section to a circuit, said output virtual channel cell rate control section feeding back the cell number to said input virtual channel cell rate control section.

4. An ATM switch as claimed in claim 1, wherein said ATM 15 core switch includes multiplexing means for multiplexing cells from all of said output side circuit interface sections, filter means for comparing output port identification numbers applied to the cells with output port numbers of said filter means themselves and passing therethrough only those cells which 20 exhibit coincidence in the comparison, and a cell buffer of the first-in first-out type provided for each output port for temporarily storing those cells which have passed through the corresponding filter means, converting the rate of the cells and outputting the resulting cells to a corresponding one of 25 said output side circuit interfaces.

5. An ATM switch as claimed in claim 2, wherein said input

cell rate control section stores an input circuit number, a service class, a minimum cell rate, an output switch port number and an intra-switch connection identification number of contents of a contract concluded in advance in a corresponding 5 relationship to a virtual path identifier/virtual channel identifier of an input cell.

6. An ATM switch as claimed in claim 3, wherein said output virtual channel cell rate control section stores a service class, a virtual channel minimum cell rate, a virtual channel peak 10 cell rate, a virtual path peak cell rate, an output circuit number and an output virtual path identifier/virtual channel identifier of contents of a contract concluded in advance in a corresponding relationship to an intra-switch connection identification number of each cell.